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## WE CLAIM:

1. A method of performing software performance analysis for a target machine, comprising: describing a system design as a network of logical entities; selecting at least one of the logical entities for a software implementation;

synthesizing a software program from the logical entities selected for the software implementation;

compiling the software program to generate an optimized assembler code representation of the software program;

performing a performance analysis using the assembler code; generating a software simulation model using the assembler code; and generating a hardware/software co-simulation model using the software simulation model.

- 2. The method of claim 1, wherein the compiling step further comprises incorporating a description of the target machine.
- 3. The method of claim 1, wherein the software simulation model is an assembler-level C code simulation model.
- 4. The method of claim 1, further comprising selecting at least one of the logical entities for a hardware implementation, and synthesizing a software model of the hardware implementation from the selected logical entities, wherein the hardware/software cosimulation model is generated using the software model of the hardware implementation.
- 5. The method of claim 1, wherein the performance analysis measures an execution time of an element of the assembler code.
- 6. The method of claim 1, wherein the software program is compiled using the same compiler used to compile a production executable.
- 7. The method of claim 1, wherein performing the performance analysis comprises annotating the assembler code with performance information.
  - 8. The method of claim 7, wherein the performance information is timing information.